REMARKS

In response to Official Action mailed November 22, 2002, Applicant amends his application and requests reconsideration. In this Amendment, no claims are added or cancelled so that claims 1-18 remain pending.

Claims 10-13 are allowed. Claim 12 is amended to ensure that all terms have proper antecedent basis. Claims 10-12 are amended for clarity and to conform to the amendments of other claims for the reasons explained below.

Claims 2 and 3 were objected to but not rejected. A limitation that appeared in both claims 2 and 3 has been moved into claim 1, namely that the semiconductor substrate includes at least one DRAM region and one logic region. An important feature of the invention is that a layer common to both of these regions is employed as a shielding layer in the logic region and as a different element within the DRAM region. For example, that metallic layer that is the shielding layer in the logic region may be used to form a bit line layer, a plate of a capacitor, or a gate electrode layer in the DRAM region. All claims have been clarified in this regard by referring to the layer as a metallic layer since it functions as an electromagnetic shield only in the logic region. Claims 8, 17, and 18, like claims 2 and 3, were objected to but not rejected. Therefore, further comment on those claims is not necessary.

Claims 1, 4, 5, and 9 were rejected as unpatentable over the prior art illustrated in Figures 6A and 13 of the patent application in combination with Sakai et al. (U.S. Patent 4,377,819). This rejection is respectfully traversed.

An important feature of the invention brought out in amended claim 1 is that a common metallic layer is present in both the DRAM region and the logic region and has different functions within each region. As conceded in the rejection, there is no layer acting as a shielding layer in the prior art structure of Figure 13 of the patent application. It is the Examiner's view that Sakai's Figures 9 and 10 illustrates a shielding layer shielding a resistor 90. Assuming, for the sake of argument, that that assertion is correct, there is still no suggestion in the prior art that if a shielding layer, like that of Sakai, were employed in the logic region of the structure of Figure 13, that the metallic layer forming the shield should continue into the DRAM region where the metallic layer has a function other than as a shielding layer. Neither of the prior art figures described in the patent application or Sakai disclose these elements of claim 1. Therefore, there is no suggestion in any potential combination of those two sources of prior art for amended claim 1. Thus, claim 1 and its dependent claims 2-4 should now be allowed.

Claim 5 is also an independent claim. Claim 5 was rejected on the same basis as claim 1, namely the prior art described in the patent application in combination with Sakai. Amended claim 5, like amended claim 1, describes a semiconductor device including at least one DRAM

region and one logic region and in which a metallic layer extends through both regions, with the metallic layer being a shielding layer in the logic region and a signal interconnection layer in the DRAM region. For the reasons already submitted with respect to claim 1, which are equally applicable with respect to claim 5, the elements of claim 5 and of its dependent claim 9 are not present in any potential combination of the prior art figures of the application or Sakai. Thus, this rejection should be with respect to claim 5.

Claim 5 was rejected as anticipated by Figure 13 of Iwasa (U.S. Patent 5,686,746). This rejection is respectfully traversed. Neither Figure 13 nor any other figure of Iwasa describes a semiconductor device including a DRAM region and a logic region in which signal interconnection layer in a DRAM region is common with a shielding layer in a logic region, as in the structure of amended claim 5. Thus, the rejection should be withdrawn.

Claim 5 and its dependent claim 9 were rejected as anticipated by Wolfrum et al. (U.S. Patent 3,373,323, hereinafter Wolfrum). This rejection is respectfully traversed.

In making the rejection, the Examiner directed attention to Figures 1 and 3 of Wolfrum, figures showing a transistor structure including leads 13 and 14. Like Iwasa, Wolfrum lacks a DRAM region and a logic region on a single semiconductor substrate. There is no common metallic layer that is a shield in one of the regions and a signal interconnection in the other region. Accordingly, the rejection should be withdrawn.

Claim 5 and its dependent claim 7 were rejected as anticipated by the prior art described in the application with respect to Figures 6A and 14. This rejection is respectfully traversed. Neither of those cited figures depicts a structure including a metal layer present commonly in both the DRAM and logic regions, that is continuous in the logic region to function as a shield and processed to be a interconnection layer in the DRAM region. Thus, the rejection should be withdrawn.

Claim 5 and its dependent claim 6 were rejected as anticipated by the prior art described in the patent application with respect to Figures 6A and 14. This rejection is respectfully traversed. In making this rejection, the Examiner compared the layer 108 of Figure 14 to the shielding layer of claim 5. The layer 108 is not continuous and therefore cannot function as a shield layer. Thus, the comparison is inaccurate and the rejection should be withdrawn, particularly as to the amended claims.

Claims 14-18 are method claims that describe a method of making a structure including two shielding layers. Claim 14 has been amended to make clearer that two shielding layers are formed in separate steps and that between the formation of the two shielding layers the signal interconnection layer is formed. Claim 16 has been clarified. A lack of antecedent basis for a term in claim 17 is corrected and other changes are made in claims 15 and 18 to conform to the amendment of claim 14.

Claims 14-16 were rejected as anticipated by the prior art described in the patent application. These rejections, appearing in three different forms, are all respectfully traversed. Figure 14 does not illustrate a structure nor suggest the method of making a structure including a signal interconnection layer sandwiched by two shielding layers. The rejection of claim 16 is moot in view of the correction of that claim. Claims 17 and 18 were stated to be allowable. Therefore, for the reasons supplied, all of method claims 14-18 are now in form for allowance.

Prompt issuance of a Notice of Allowance with respect to claims 1-18 as now pending is earnestly solicited.

Respectfully submitted,

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JAW/tph

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Shinya SOEDA

Application No. 10/077,767 Art Unit: 2811

Filed: February 20, 2002 Examiner: M. Prenty

For: SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME

AMENDMENTS TO CLAIMS
MADE IN RESPONSE TO OFFICE ACTION DATED NOVEMBER 22, 2002

Amendments to existing claims:

1. (Twice Amended) A semiconductor device comprising:

a semiconductor substrate having ~~a plurality of regions~~ at least one DRAM region and one logic region;

a resistor group including a plurality of resistors located in ~~one of~~ said ~~regions of said semiconductor substrate~~ logic region;

a metal interconnection layer opposite ~~the region in which~~ said resistor group ~~is located~~ in said logic region; and

a ~~shielding~~ metallic layer disposed between said resistor group and said metal interconnection layer in said logic region as a shielding layer and partially disposed within said DRAM region.

2. (Twice Amended) The semiconductor device according to claim 1, ~~comprising at least one DRAM region and at least one logic region, including a~~ wherein said metallic layer ~~common to~~ is a bit line layer in said DRAM region ~~and use as a shielding layer in said logic region~~.

3. (Twice Amended) The semiconductor device according to claim 1, comprising ~~at least one DRAM region with a stacked capacitor and one logic region, wherein said~~ a stacked capacitor in said DRAM region ~~includes~~ and including a lower capacitor electrode layer, a dielectric film, and an upper capacitor electrode layer, ~~and a layer common to~~ said

upper capacitor electrode layer ~~in said DRAM region and used as~~ being part of said ~~shielding~~ metallic layer ~~in said logic region~~.

5. (Twice Amended) A semiconductor device comprising:

a semiconductor substrate having at least one DRAM region and one logic region;

a signal interconnection layer ~~on~~ in said ~~semiconductor substrate~~ logic region; and

a ~~shielding~~ metallic layer in said DRAM region and said logic region and located on ~~at least~~ one side of said signal interconnection layer, with respect to said semiconductor substrate, as a shielding layer in said logic region.

6. (Twice Amended) The semiconductor device according to claim 5, wherein said metallic layer is a gate electrode layer in said DRAM region ~~and used as said shielding layer in said logic region~~.

7. (Twice Amended) The semiconductor device according to claim 5, ~~comprising at least one DRAM region and one logic region, including a layer common to~~ wherein said metallic layer is a bit line layer in said DRAM region ~~and used as said shielding layer in said logic region~~.

8. (Twice Amended) The semiconductor device according to claim 5, comprising ~~at least one DRAM region with a stacked capacitor and one logic region, wherein said~~ stacked capacitor in said DRAM region ~~includes~~ and including a lower capacitor electrode layer, a dielectric film, and an upper capacitor electrode layer, ~~and a layer common to~~ said upper capacitor electrode layer in said DRAM region ~~and used as~~ being part of said ~~shielding~~ metallic layer ~~in said logic region~~.

10. (Twice Amended) A method of fabricating a semiconductor device having at least one DRAM region and one logic region and having a resistor group in said logic region, the method comprising:

forming a resistor group in said logic region;

forming a ~~shielding~~ metallic layer as a shielding layer in said ~~DRAM~~ logic region and in said ~~logic~~ DRAM region; and

forming a metal interconnection layer opposite a portion of said logic region where said resistor group is located.

11. (Twice Amended) The method according to claim 10, wherein said ~~shielding~~

metallic layer is a bit line layer in said DRAM region.

12. (Twice Amended) The method according to claim 10, further comprising forming a stacked capacitor having a lower capacitor electrode layer, a dielectric film, and an upper capacitor electrode layer in said DRAM region, wherein said upper capacitor electrode layer is part of said ~~shielding~~ metallic layer.

14. (Twice Amended) A method of fabricating a semiconductor device having at least one DRAM region and one logic region and having a signal interconnection layer in said logic region, the method comprising:

forming a first metallic layer as a first shielding layer in said logic region and in said DRAM region;

forming a signal interconnection layer in said logic region opposite said first shielding layer; and

forming a second metallic layer as a second shielding layer ~~on at least one side of~~ opposite said signal interconnection layer in said ~~DRAM region and said~~ logic region and in said DRAM region.

15. (Amended) The method according to claim 14, wherein one of said ~~shielding~~ first and second metallic layers is a gate electrode layer in said DRAM region.

16. (Amended) The method according to claim 14, wherein one of said ~~shielding~~ first and second metallic layers is a bit line layer in said DRAM region.

17. (Twice Amended) The method according to claim 14, further comprising forming a stacked capacitor having a lower capacitor electrode layer, a dielectric film, and an upper capacitor electrode layer in said DRAM region, wherein said upper capacitor electrode layer in said DRAM region is part of said second ~~shielding~~ metallic layer.

18. (Twice Amended) The method according to claim 14, further comprising fixing potential of one of said first and second shielding ~~layer~~ layers.